

#1  
end

9 interrupt circuitry cooperatively designed with the instruction pipeline circuitry to  
 10 synchronously trigger an interrupt in accordance with interrupt criteria on execution of an  
 11 instruction of a process, wherein the architectural definition of the instruction does not call  
 12 for an interrupt, the interrupt criteria being based at least in part on the table entry associated  
 13 with the address of the instruction, the interrupt circuitry being designed to invoke a handler  
 14 for the interrupt, the handler being responsive to a content of the table entry to affect the  
 15 instruction pipeline circuitry to effect control of an architecturally-visible data manipulation  
 16 behavior or control transfer behavior of the instruction based on the contents of a table entry  
 17 associated with the address range in which the instruction lies.

Kindly add the following new claim:

#2

1 ~~81.~~ (new August 27, 2002) A microprocessor chip, comprising:  
 2 instruction pipeline circuitry; and  
 3 table lookup circuitry designed to retrieve an entry from a table, each entry of the  
 4 table being associated with a corresponding address range of an address space translated by  
 5 address translation circuitry of the microprocessor chip, each entry describing a likelihood of  
 6 the existence of an alternate coding of instructions located in the respective corresponding  
 7 address range, the table lookup circuitry operable as part of the basic instruction cycle of  
 8 executing an instruction of a non-supervisor mode program for execution on the  
 9 microprocessor chip, the table being stored in storage that is architecturally invisible to  
 10 programs in the native architecture of at least some instructions executed by the  
 11 microprocessor chip;  
 12 interrupt circuitry cooperatively designed with the instruction pipeline circuitry to  
 13 trigger a synchronous interrupt on execution of an instruction of a process, wherein the  
 14 architectural definition of the instruction of the process does not call for an interrupt, a trigger  
 15 for the interrupt being synchronously based at least in part on the table entry corresponding  
 16 to the address of the instruction of the process, the interrupt circuitry being designed to  
 17 invoke a handler for the interrupt, the handler being responsive to a content of the table entry  
 18 to affect the instruction pipeline circuitry to effect control of an architecturally-visible data  
 19 manipulation behavior or control transfer behavior of the instruction of the process, based at